A 500MHz 1.5 MByte Cache with On-Chip CPU

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Outline

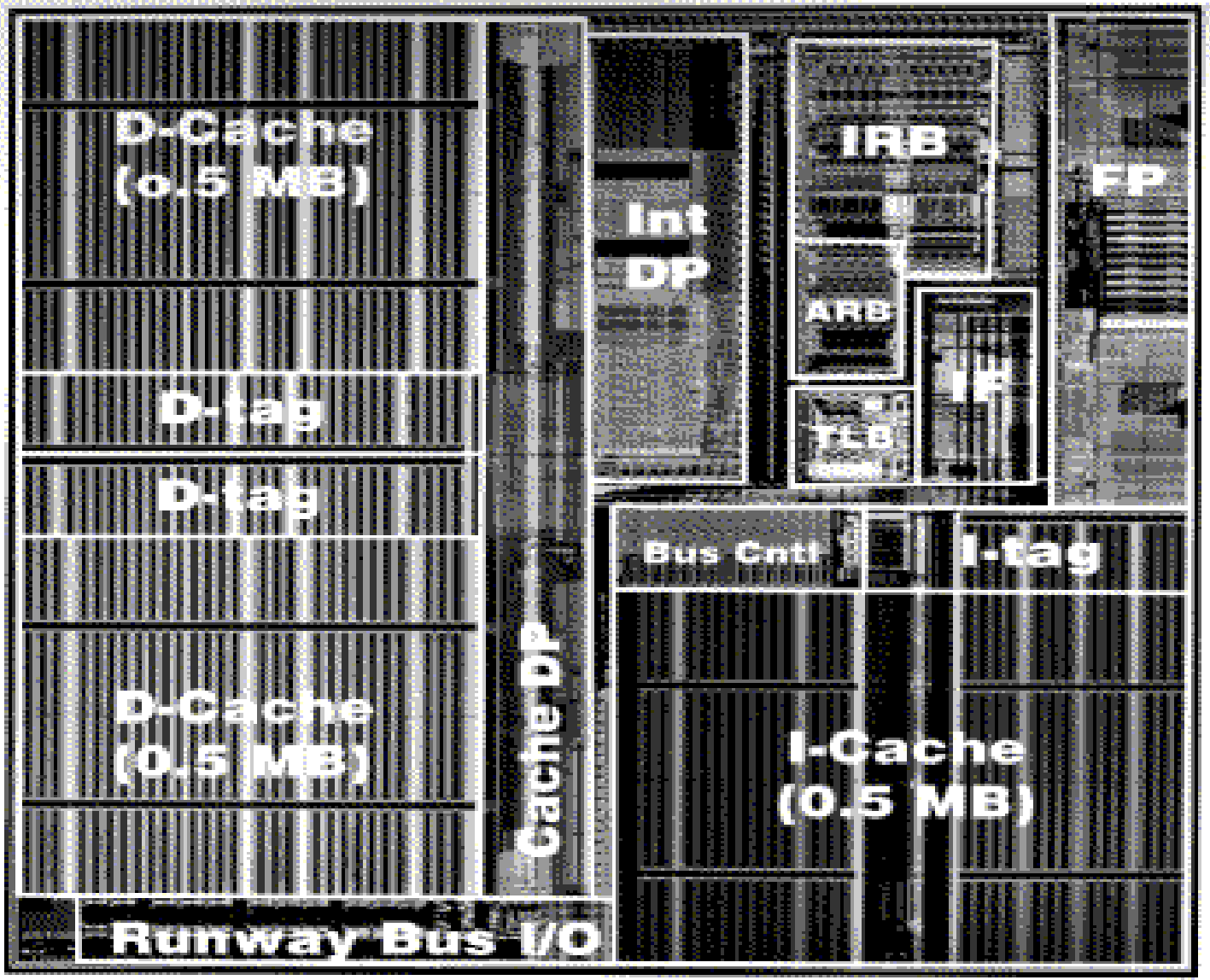
- Technology
- Cache Architecture
- Timing Control
- Address Paths
- Write Path
- Read Path
- Redundancy
- Performance
- Conclusions

Technology

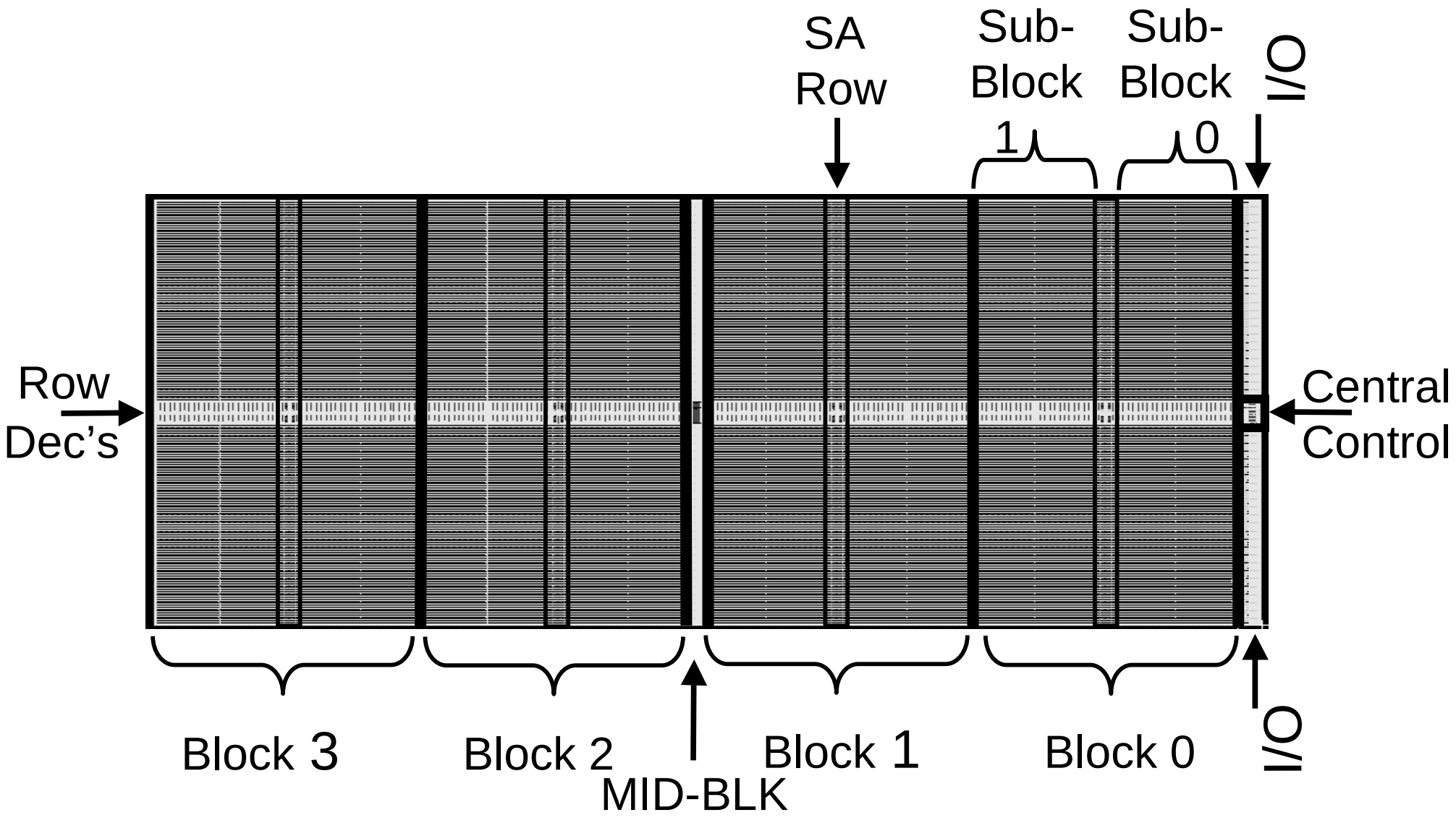
- 0.25um CMOS
- 5 levels of Al interconnect
- Sub-12 square micron memory cell

  I_{cell} = 130uA at 110 Degrees C, 1.6v

Die Photo


D-Cache
(0.5 MB)
D-tag
D-tag
D-Cache
(0.5 MB)
Cache DP
Runway Bus I/O
Int
DP
IRB
ARB
TLB
FP
Bus Cntl
I-tag
I-Cache
(0.5 MB)

1/4 MBYTE D-CACHE DATA STACK



BLOCK ARCHITECTURE

SUB-BLOCK 1		SUB-BLOCK 0
256 x 4, N	MCL	256 x 4, N
• • •	• • •	• • •
256 x 4, 1	MCL	256 x 4, 1
256 x 4, 0	MCL	256 x 4, 0
ROW DEC'S	MID CNTL	ROW DEC'S
256 x 4, 0	MCL	256x 4, 0
256 x 4, 1	MCL	256 x 4, 1
• • •	• • •	• • •
256 x 4, N	MCL	256 x 4, N

MCL

Left and Right:

BIT PRECHARGE

READ COL MUX

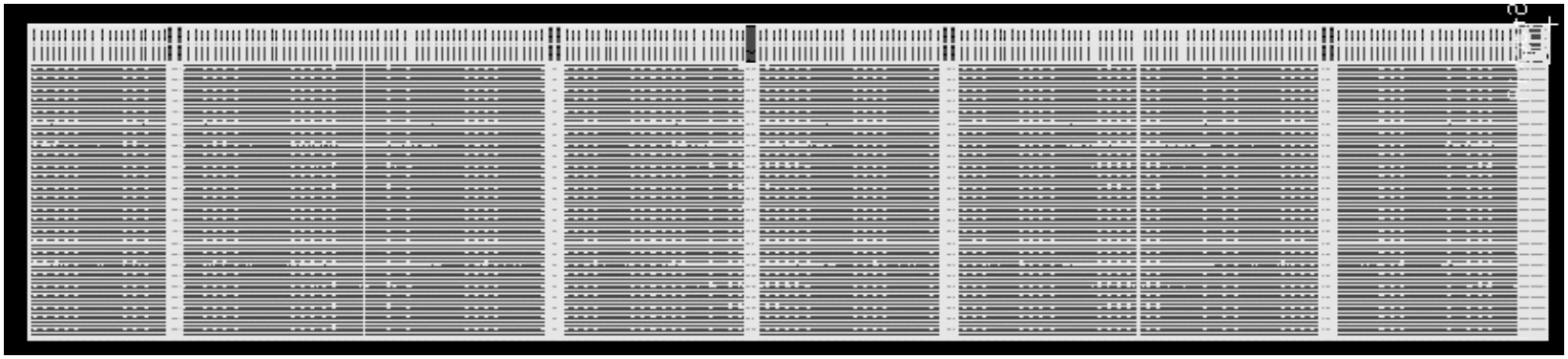
WRITE COL MUX

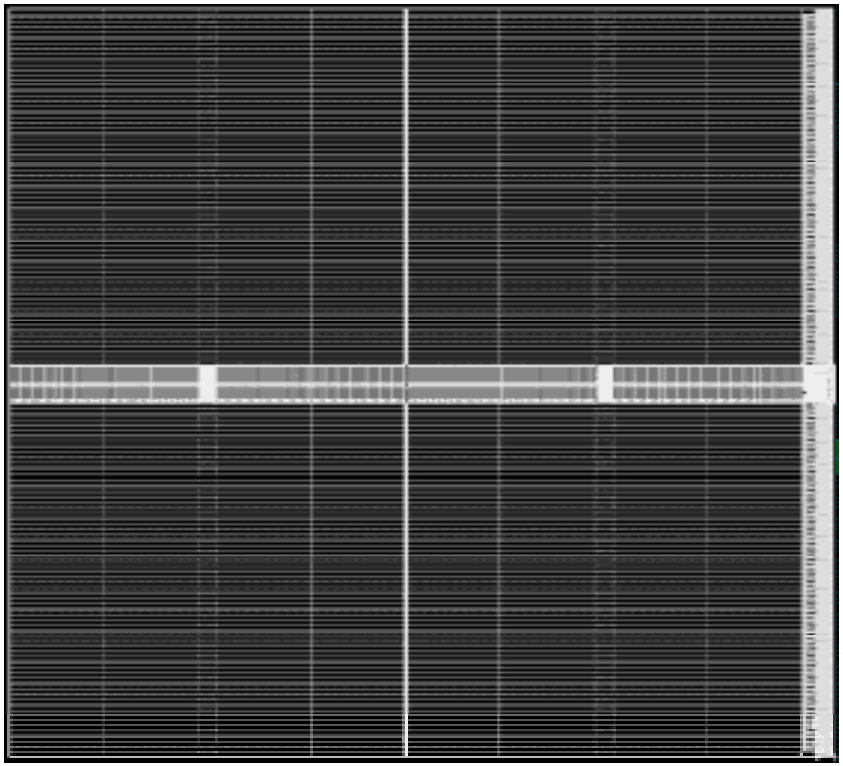
Shared:

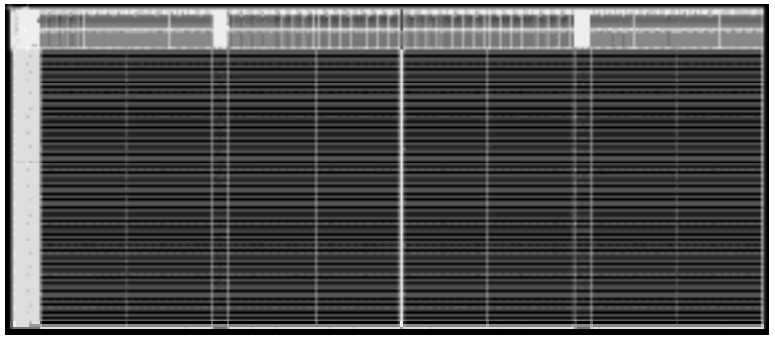
SENSE-AMP

COL PRECHARGE

128KB D-CACHE TAG





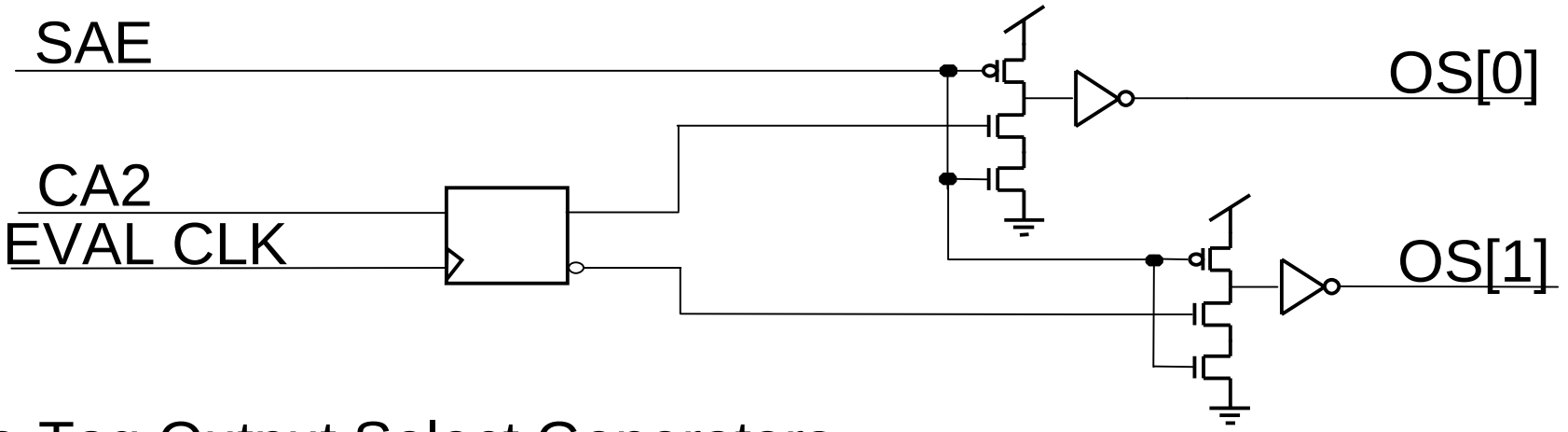


64KB I-CACHE TAG

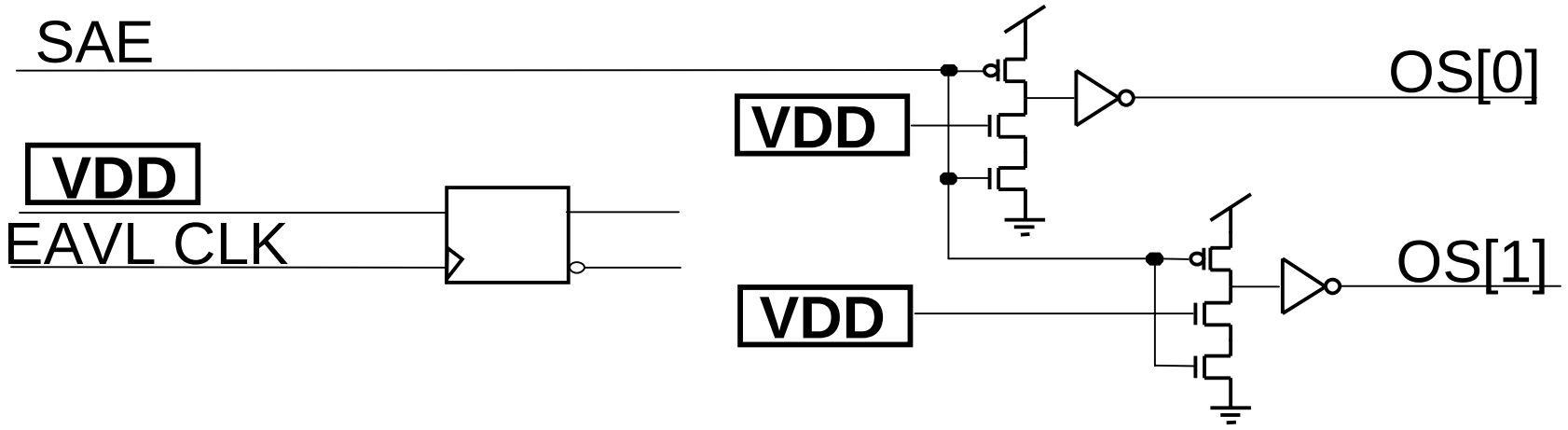
128KB I-CACHE DATA

BLOCK COMMONALITY TECHNIQUE

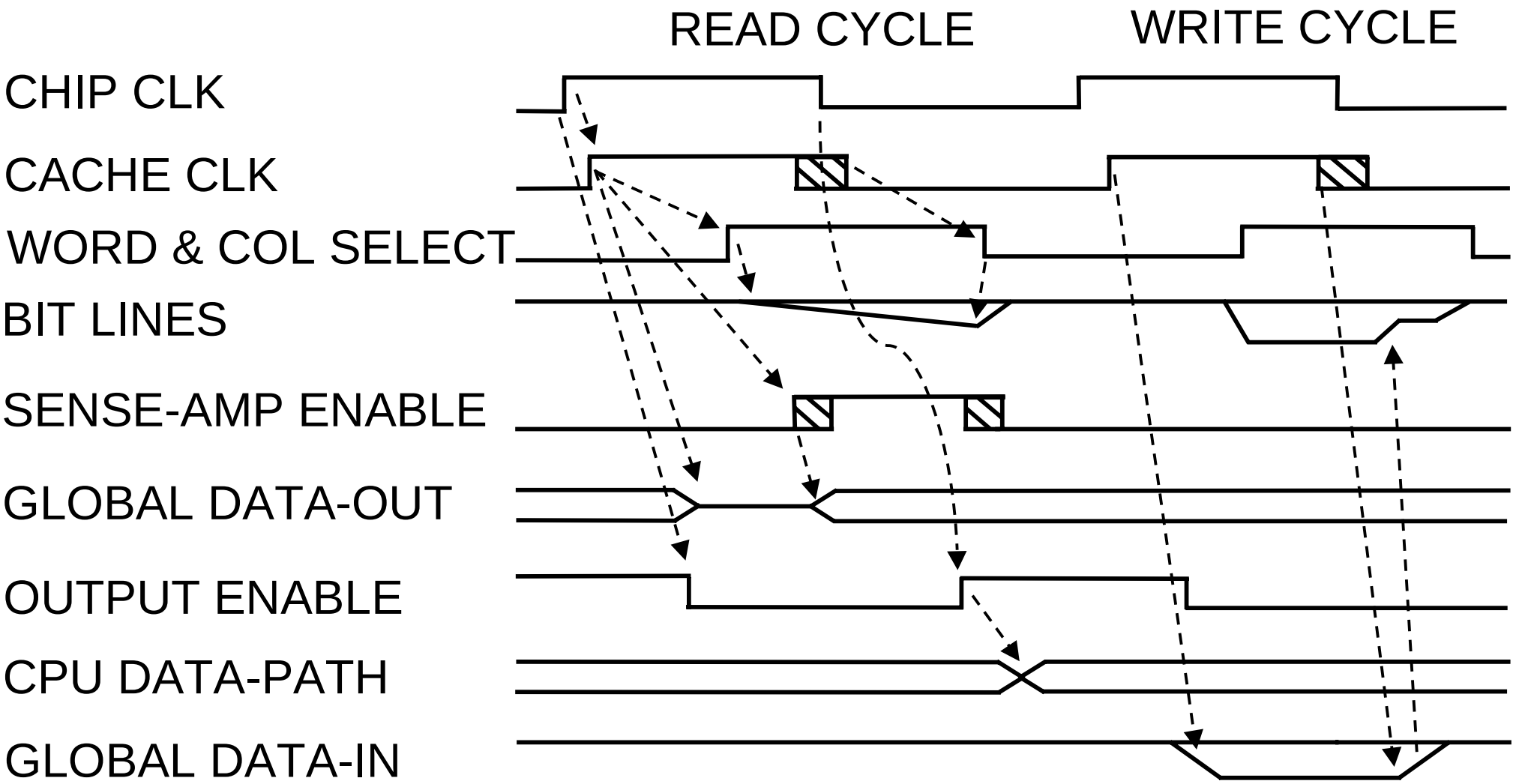
Data-Data Output Select Generators



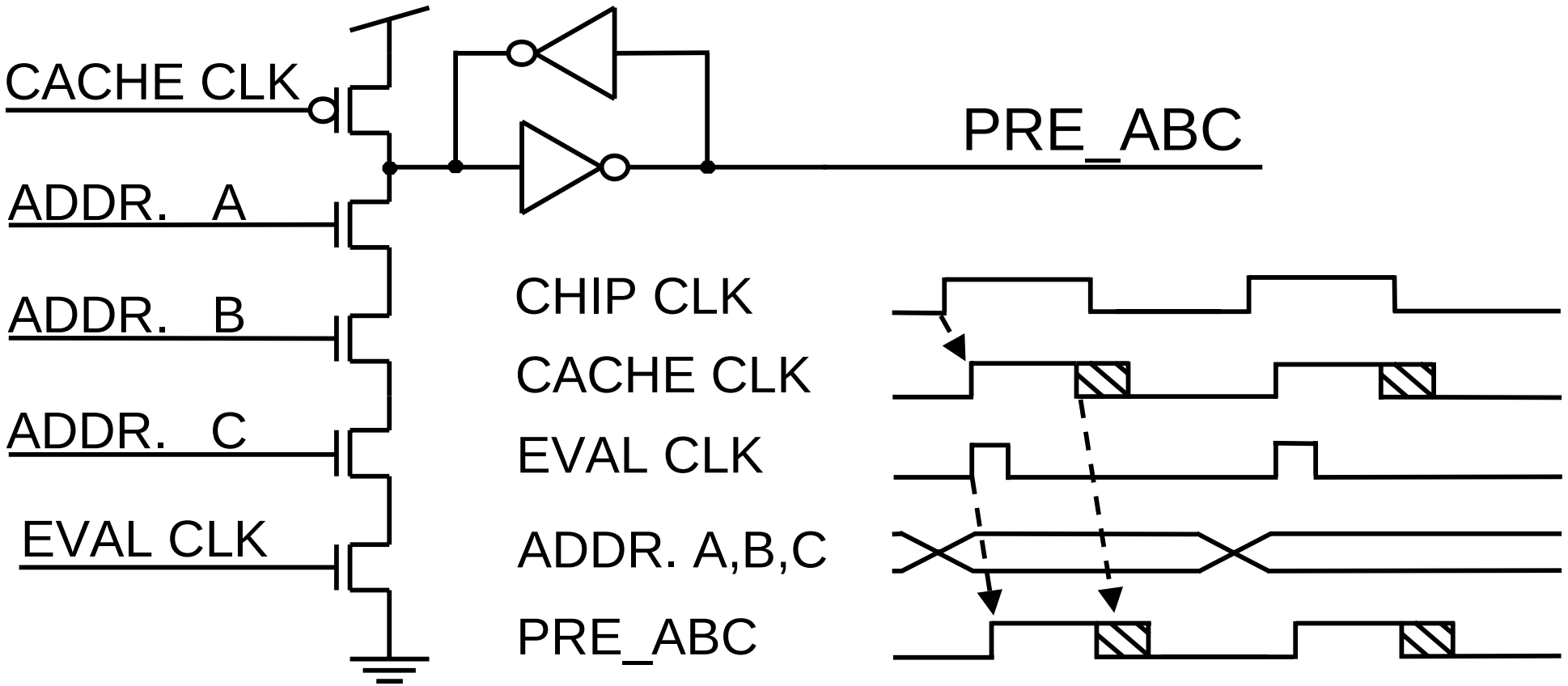
Data-Tag Output Select Generators



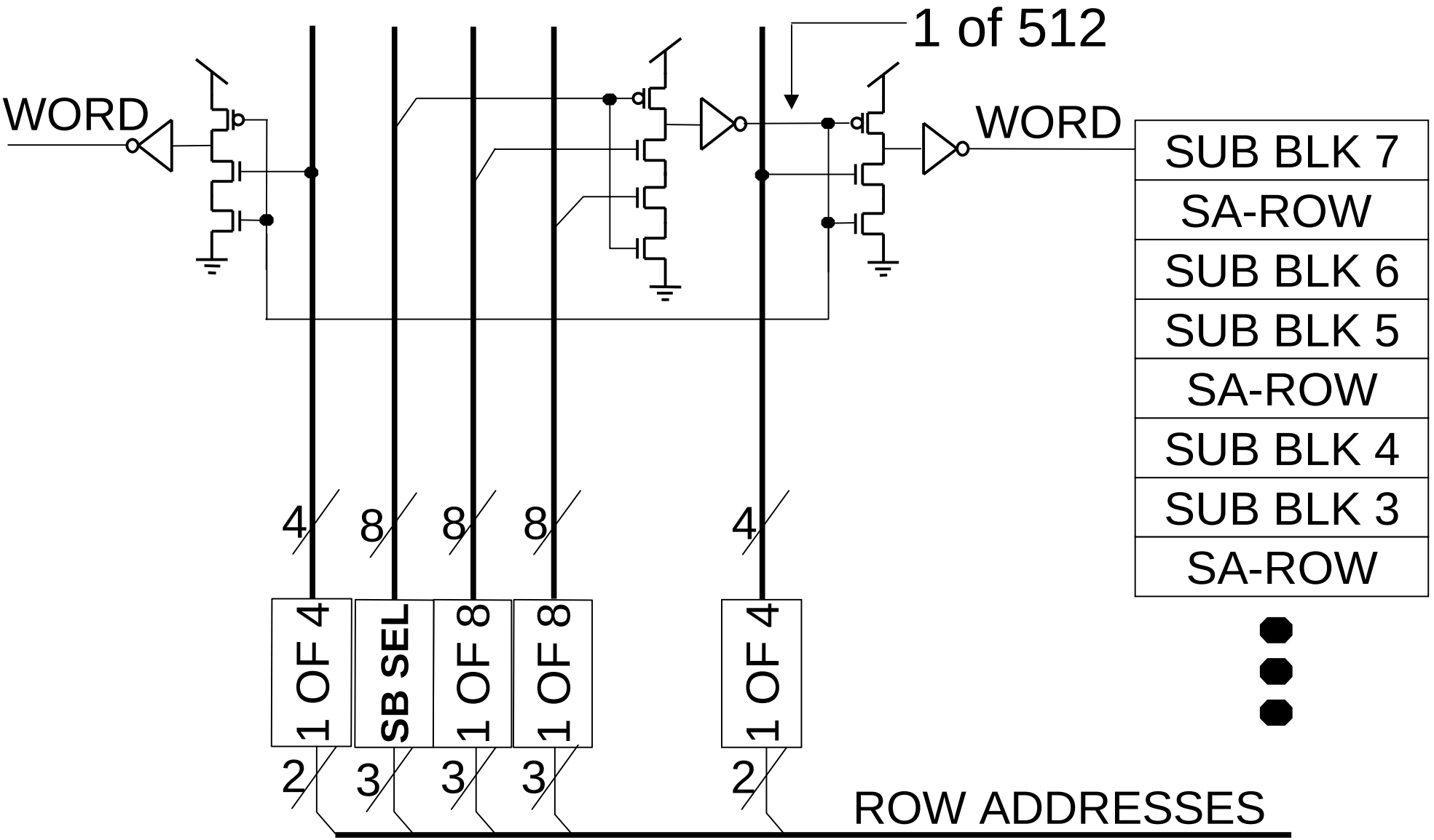
TIMING CONTROL



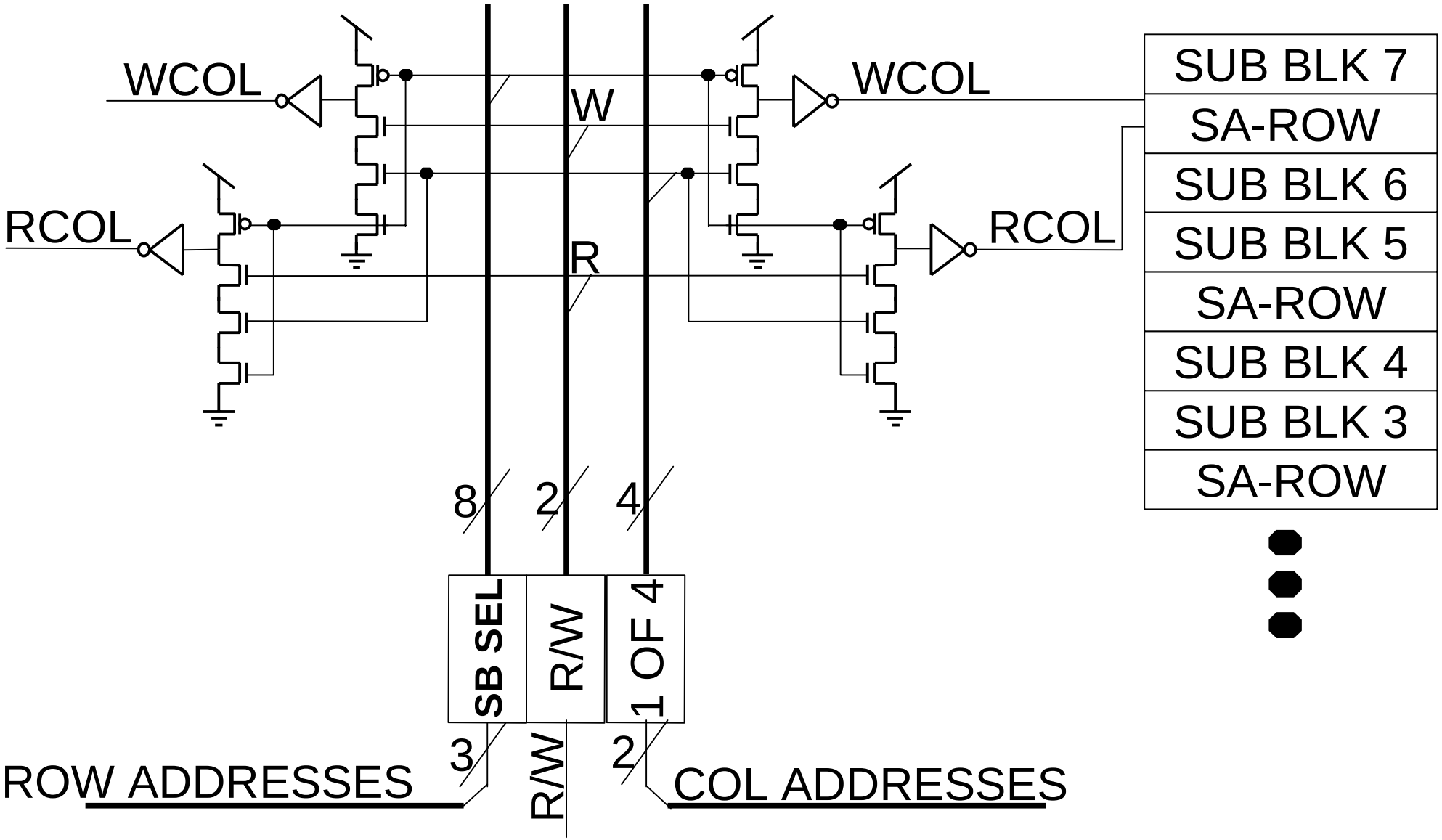
ADDRESS AND CONTROL PRE-DECODE



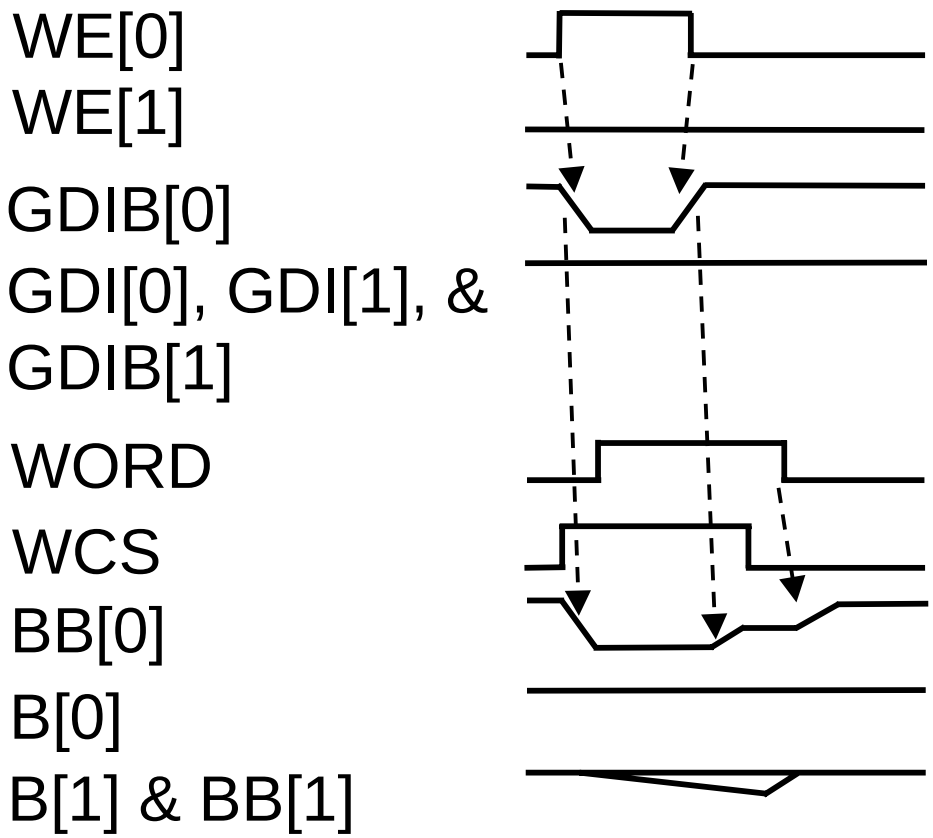
ROW ADDRESS DECODING

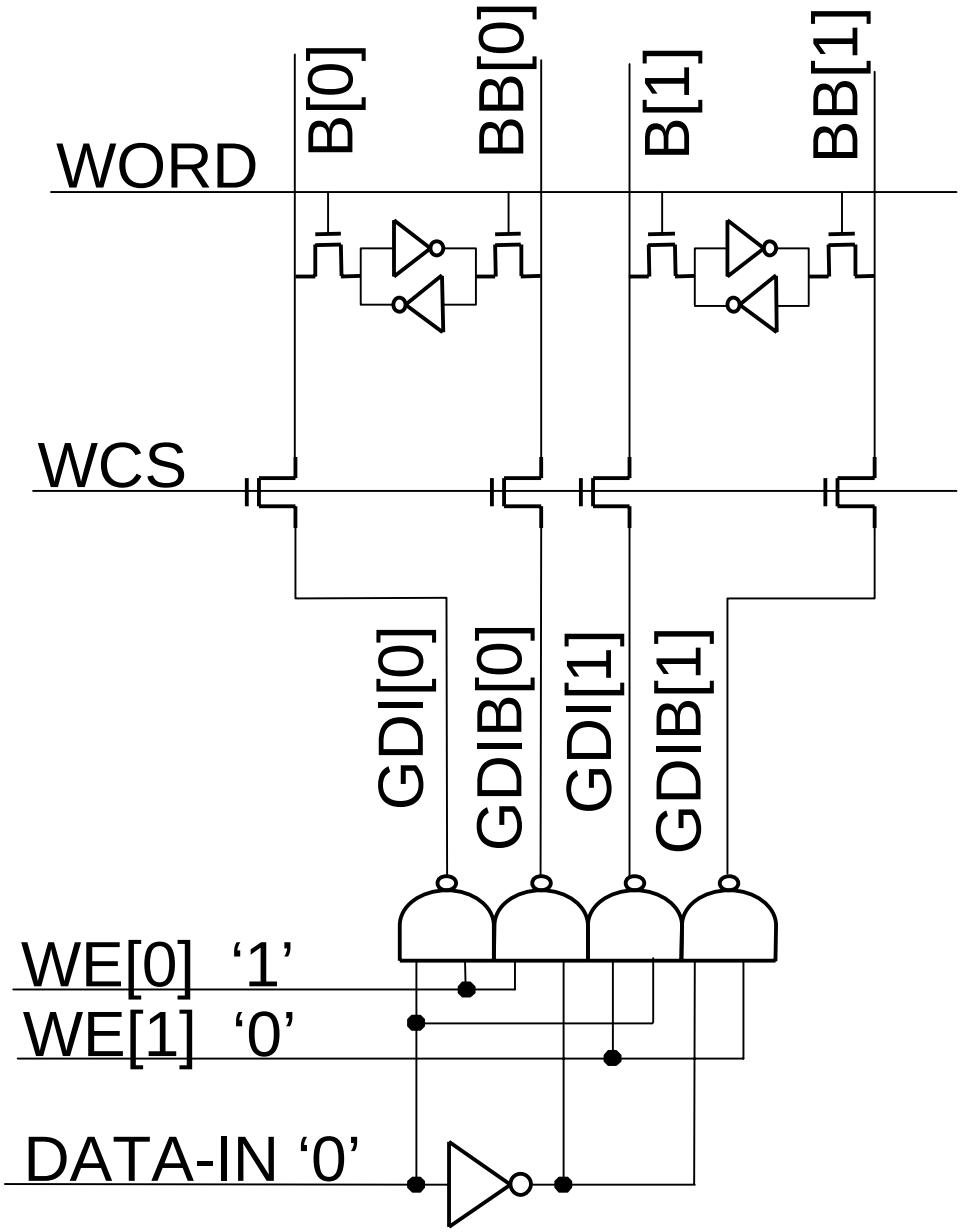


COLUMN DECODING

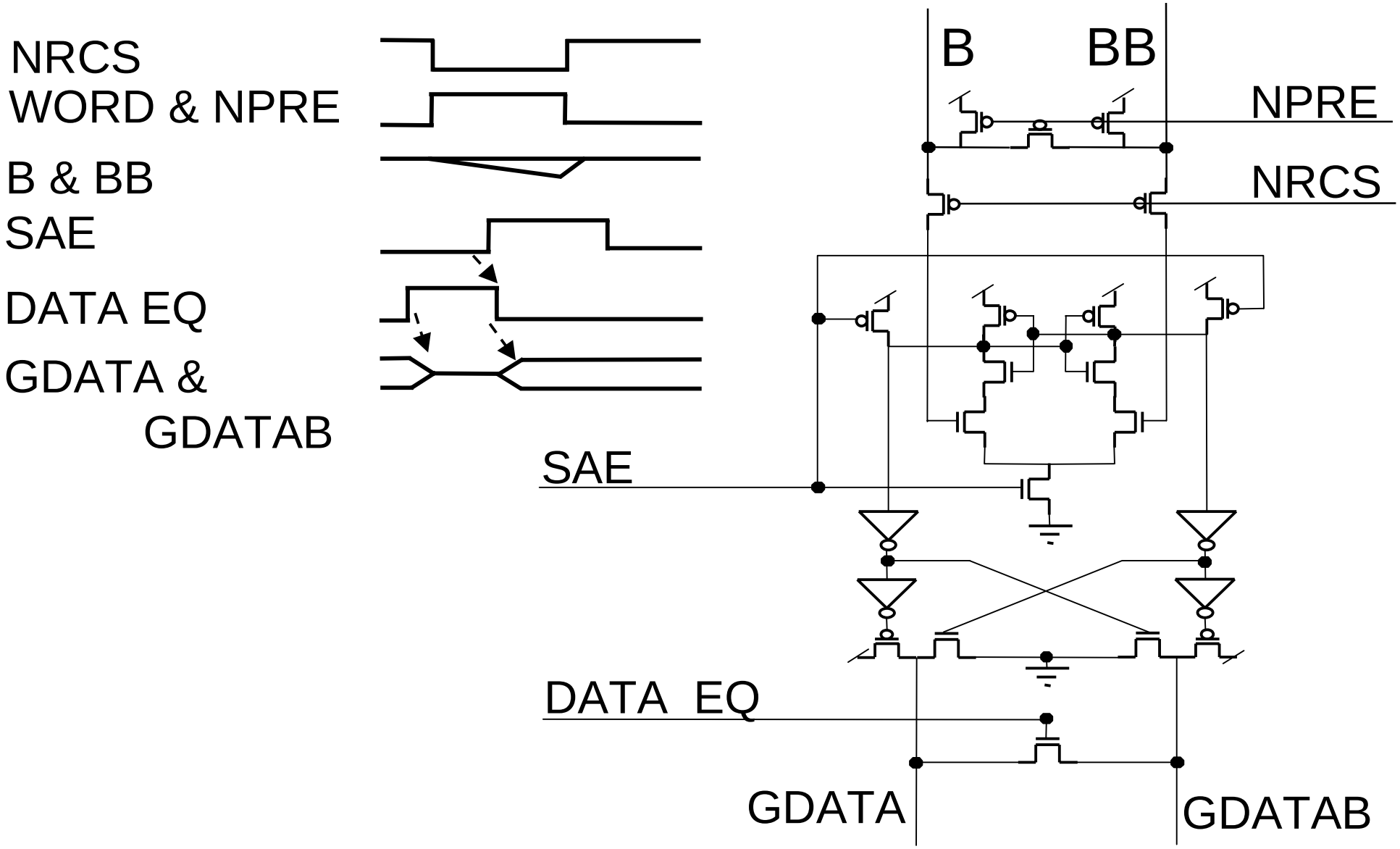


WRITE PATH

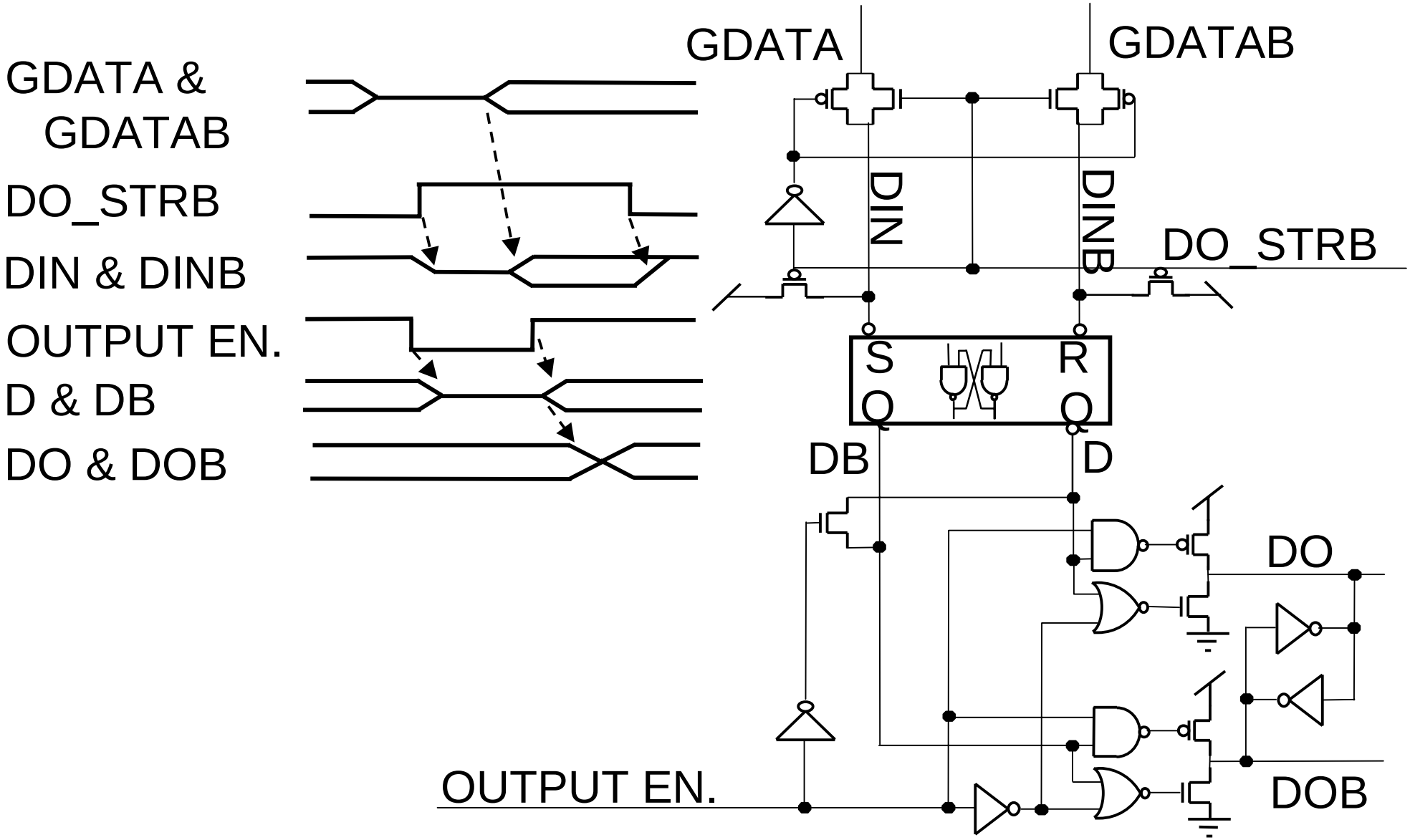

WE[0]
WE[1]
GDIB[0]
GDI[0], GDI[1], &
GDIB[1]
WORD
WCS
BB[0]
B[0]
B[1] & BB[1]


B[0]
BB[0]
B[1]
BB[1]
WORD
WCS
GDI[0]
GDIB[0]
GDI[1]
GDIB[1]
WE[0] ‘1’
WE[1] ‘0’
DATA-IN ‘0’

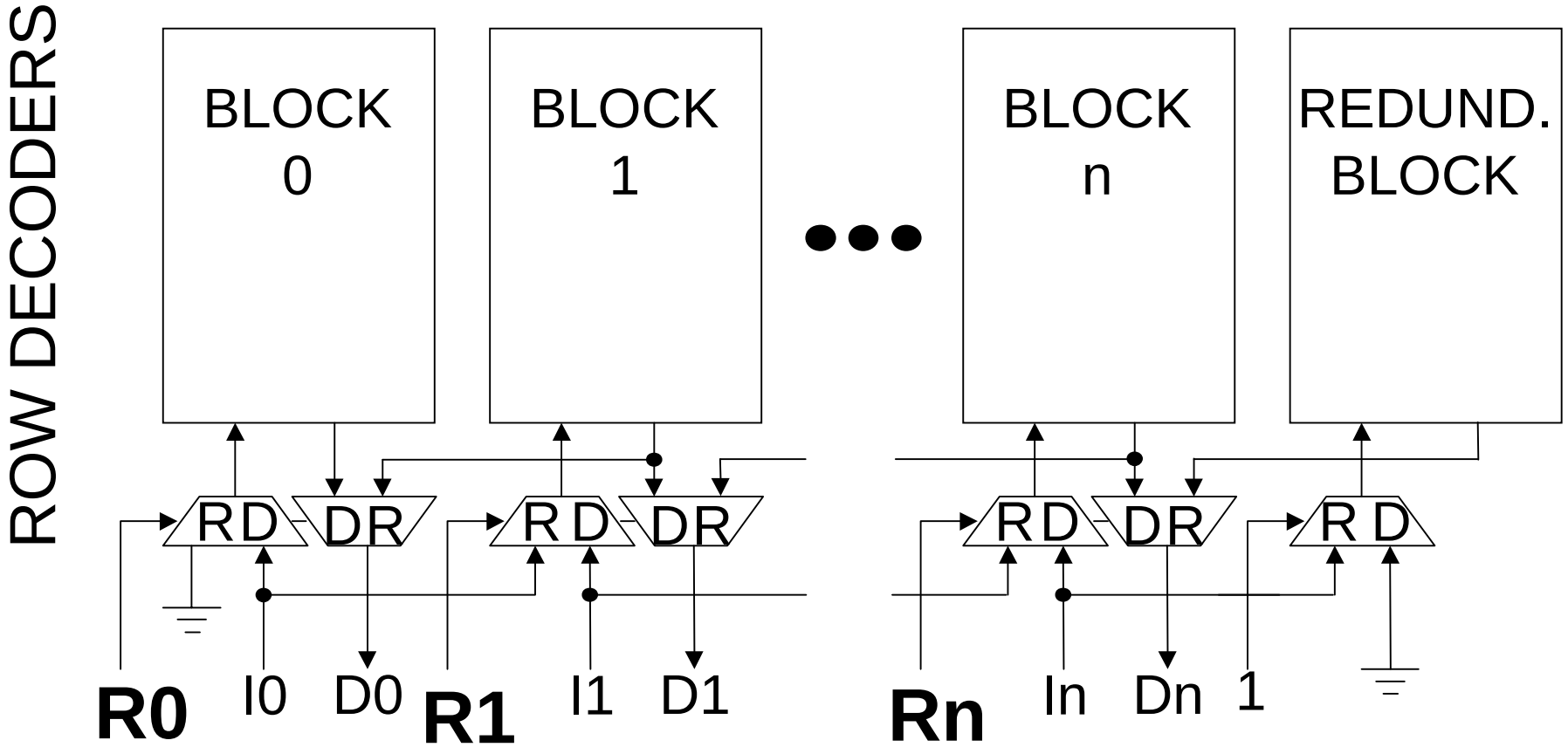
THE SENSE-AMP



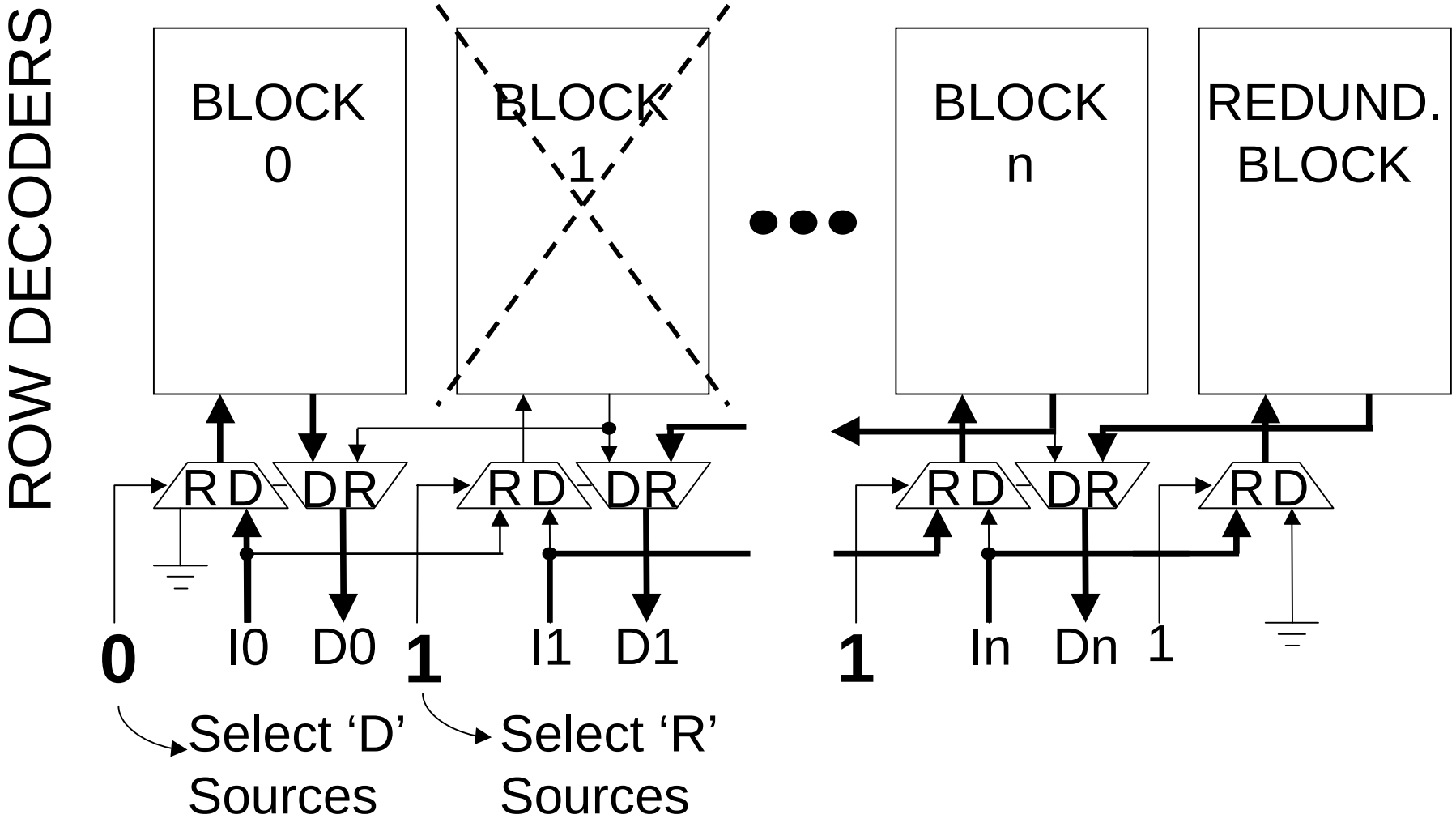
THE OUTPUT BUFFER



REDUNDANCY DATA STEERING

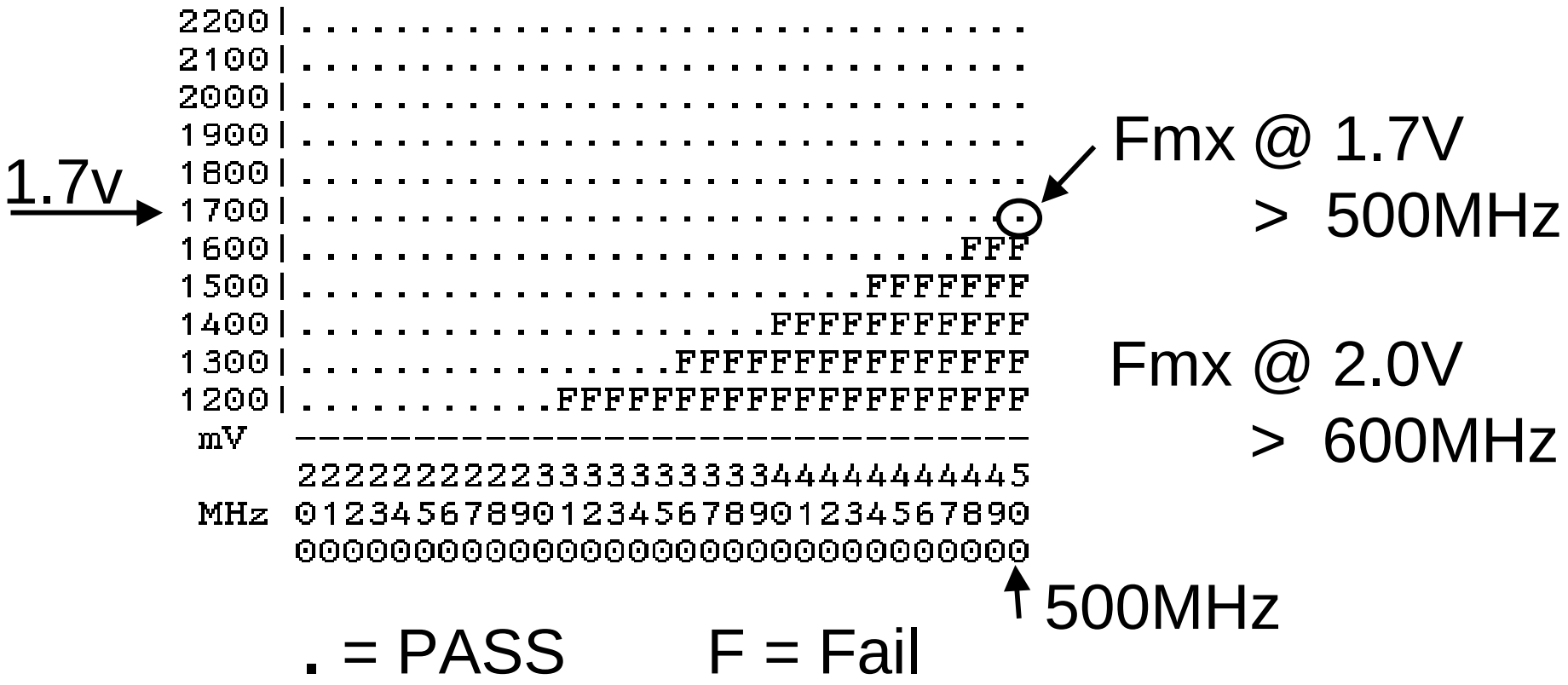


REDUNDANCY DATA STEERING EXAMPLE



Performance

Nominal Silicon
50 Degrees Celsius



Conclusions

- Combining:
  - 0.25um technology
  - Data Driven Address Path
  - Low Skew Control Signal
  - Fully Differential Data Paths

- Yields:
  - 1.5 Mbytes
  - Greater than 500MHz Operation
  - Consuming < 12.5W @ 2.0V, 500MHz