PA-RISC 2.0 Firmware Architecture Reference Specification

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A. Glossary

Accessible

An address or address range is **Accessible** if an attempt to read or write to it does not generate an addressing error.

Architected

A facility, address, or functionality is **Architected** if it is one which must be implemented by a module for the module to be considered architecturally compliant.

Boot

Boot is one way that a native processor can respond to reset or power-on. The result of boot is that the system is forced into an initial state and the Initial Program Load (IPL) is obtained from the boot device and executed.

Boot Device

The **Boot Device** is the input device from which PDC obtains the Initial Program Load (IPL). The boot device must be a sequential or random access device and must contain a properly formatted IPL image.

Boot Module

The **Boot Module** is the module to which the boot device is attached. PDC locates the boot module during boot based on the contents of Stable Storage, searching, or operator input.

Broadcast Interrupt

A **Broadcast Interrupt** is an external interrupt message (EIM) sent to an external interrupt request (EIR) register in the broadcast address space. If the external interrupt message is sent to the Local Broadcast Address Space, it applies to all processor modules on the local bus; this is called a **Local Broadcast Interrupt**. If the external interrupt message is sent to the Global Broadcast Address Space, it applies to all processor modules in the system; this is called a **Global Broadcast Interrupt**.

Broadcast Physical Address (BPA) Space

The **Broadcast Physical Address Space** or **BPA Space** consists of the range of addresses from 0xFFFFFFFF FFFC0000 through 0xFFFFFFFF FFFFFFFF. This space is divided up into the Local Broadcast Address Space (0xFFFFFFFF FFFC0000 through 0xFFFFFFFF FFFDFFFF) and Global Broadcast Address Space (0xFFFFFFFF FFFE0000 through 0xFFFFFFFF FFFFFFFF).

Broadcast Transaction

A **Broadcast Transaction** is a WRITE4 transaction whose SADD phase maps to an address in the broadcast address space. Broadcast transactions to the local broadcast address space and the global broadcast address space are termed **Local Broadcast Transactions** and **Global Broadcast Transactions**, respectively.

Bus Category

The **bus category** defines the kind of algorithm needed on the bus to guarantee cache and TLB coherence on the bus.

Bus Specification

A **bus specification** specifies the electrical and physical characteristics of a bus. It also defines which optional portions of the connect protocol have been implemented and defines how the connect protocol has been implemented.

Cacheable Page

A **Cacheable Page** is a page in the memory or PDC address space which must be accessed only with a burst operation. Data from these pages may be placed in cache lines within processor modules.

Category A Bus

Category A busses require software participation to guarantee cache and TLB coherence. Category A busses only allow the coexistence of category A modules.

Category A Module

Category A modules do not participate in any software-independent coherence algorithm. As masters, category A modules may only issue transaction modes supported by category A busses. As slaves or transaction third parties, category A modules are required to alias all transaction variants to the corresponding default transaction variant.

Category B Bus

Category B busses support cache and TLB coherence between modules on the same bus without software participation. Each category B bus defines its own coherence algorithm.

Category B busses must allow the coexistence of any combination of category A and B modules. The coherence algorithm, however, only supports category B modules; software participation is required to guarantee coherence on a category B bus with category A modules.

Category B Module

Category B modules participate in the software-independent coherence algorithms defined by their category B bus. As masters, category B modules are allowed to issue any of the transaction modes supported by their category B bus. As slaves or transaction third parties, category B modules are required to implement the transaction mode functionality specified by their category B bus.

Central Bus

The bus on which the processor and memory modules are located is the **Central Bus**. The central bus is the root of the tree of busses.

Check Severity

The **Check Severity** field is comprised of bits 30 and 31 in the CPU State Word for HPMC that allows OS_HPMC to determine the scope of damage. The three interpretations for the severity are defined as follows:
error critical (00) - An error has occurred which hardware determines to be non-recoverable. This may be because hardware has lost information about the error, or because there is no way to encode the error in PIM. This encoding asserts that the condition is system damaging, as well as the possible lack of storage integrity.
error transparent (01) - An error has occurred but has been fully corrected or circumvented in a way transparent to software. There must be storage integrity for this encoding to be reported. This encoding asserts the condition is repressible.
error isolated (10,11) - An error has occurred and the PIM contents can be used by OS_HPMC to determine the scope of damage and decide what recovery actions are required. There must be storage integrity for this encoding to be reported. This encoding does not imply a scope of damage. OS_HPMC must analyze other fields in PIM to determine the scope of damage.

CLEAR Transaction

A **CLEAR transaction** is the indivisible transaction which transfers data from the slave to the master and clears the first four bytes at the specified slave address.

Coherence Size

The **Coherence Size** is the granularity, in bytes, based on which cache coherence conflicts are resolved. For example, it is the amount of data which is flushed when a cache flush instruction is executed.

Complete Transaction

A **complete transaction** represents the master's successful or failed attempt to complete a transaction independent of the number of times the transaction is busied.

Connect Protocol

The **connect protocol** specifies the features that are common to all native busses. It defines features like transaction definitions, error reporting mechanisms, forward progress, arbitration algorithms, and power requirements. Software may be written to depend upon any architectural statement regarding these areas.

Console Device

The **Console Device** or **console** is the input/output device that PDC uses during boot to display messages to the operator and obtain responses from the operator. In the case of a simplex console, the console is actually composed of two devices: the display device for output and the keyboard device for input.

Deadlock

A **Deadlock** is the permanent blocking state of a set of processes/modules that require two or more specific resources or event completions, which can be provided only by other processes/modules belonging to that set.

Device

A **Device** is the object to which input and/or output operations are done. Devices are connected to but are not part of an I/O module. They are accessed directly or indirectly through the address space of that I/O module, and they may optionally be independently powered. Each I/O module may have any number of devices connected to it. For the purposes of architectural discussion, the device includes all the entities (such as cables, controllers, link adapters, etc.) between the module and the physical device. Examples of devices are terminals, disks, tape drives, and network connections.

Direct Memory Access (DMA)

An I/O module that can autonomously read and write memory is said to be performing **Direct Memory Access** or **DMA**.

Directed Interrupt

A **Directed Interrupt** is an external interrupt message which is directed to the external interrupt request register of a single processor module.

Directed Transaction

A **Directed Transaction** is a transaction whose SADD phase maps to an address in the memory, PDC, or I/O address space.

Display Device

The **Display Device** or **display** is the output device that PDC uses during boot to display messages to the operator.

Duplex Console

A **Duplex Console** is a console where the same I/O device, and the same I/O module or pseudo-module, is used for the console input and output functions.

Engineering Note

An **Engineering Note** points out information of primary interest to hardware designers.

Extended Power Failure

Extended power failure is the situation in which the duration of primary power failure is too long that secondary power eventually fails, destroying the contents of memory. In such a case, when primary power is finally restored, the system will hard boot, as recovery is not possible.

External Interrupt Message (EIM)

An **External Interrupt Message** or **EIM** is a WRITE operation sent by a module to interrupt one or more processors. The data in the EIM contains the interrupt group.

External Interrupt Request (EIR) Register

An **External Interrupt Request Register** or **EIR Register** is the destination for external interrupt messages (EIMs). The EIR contains 32 bits, one for each of the 32 interrupt groups. Only processors have an EIR register.

Field Replaceable Unit (FRU)

A **Field Replaceable Unit** or **FRU** is a part in a Precision system which is designed for replacement on the customer site. For example, a printed circuit board is often an FRU, but a component on the board is typically not.

First-Level Interrupt Handler (FLIH)

The **First-Level Interrupt Handler** or **FLIH** is the interruption handling routine for external interrupts.

Forward Progress

Forward progress is the requirement that all system operations, once desired, complete in a finite and deterministic time. Forward progress is guaranteed by avoiding module starvation and deadlock.

Generic Software

Generic software is software which is expected to communicate with a wide variety of module types. Generic software uses IODC data and entry points to determine the specific characteristics of a module. Generic software need only be changed when some drastic change in the I/O Architecture occurs, such as the addition of a new module type or the addition of fault tolerance. Examples of generic software functions are interrupt handling, powerfail preparation and recovery, error handling, and system initialization and configuration.

Global Broadcast Address Space

The **Global Broadcast Address Space** consists of addresses in the range 0xFFFFFFFF FFFE0000 through 0xFFFFFFFF FFFFFFFF.

Hard Boot

A **Hard Boot** is a boot in which memory is tested destructively. A hard boot is initiated by a broadcast CMD_RESET, or by a power-on when memory SPA contents have been lost.

Hard Physical Address (HPA)

After configuration, every module responds to a 4 Kbyte address range in the I/O address space called its **Hard Physical Address** or **HPA** space. The HPA space allows access to functionality which is architecturally required of all modules.

Hardware Version (HVERSION)

For each module, the **Hardware Version** or **HVERSION** specifies a unique hardware implementation. The *model* field of the HVERSION specifies the hardware implementation and is changed for implementations with incompatible diagnostic requirements. The *rev* field is changed for a new hardware design. For native processors HVERSION is returned by PDC_MODEL. For all other modules HVERSION is stored in the IODC_HVERSION halfword of IODC.

High-Priority Machine Check (HPMC)

A **High-Priority Machine Check** or **HPMC** is the highest priority interruption in a native processor. An HPMC indicates the detection of a hardware fault that must be handled in software before operation can continue.

HVERSION Dependent (HV)

An item in a module is **HVERSION Dependent** if its functional definition is dependent on the module's IODC_SVERSION[model] and IODC_HVERSION[model]. The HVERSION designers are free to specify the functionality, provided the definition does not conflict with any architected/module-type dependent definition.

Initial Memory Module (IMM)

The **Initial Memory Module** or **IMM** is the memory module on the central bus which is selected by PDCE_RESET to contain Page Zero, the Console Device IODC, the Boot Device IODC, and the IPL code. In the absence of failures, the Initial Memory Module is the memory module on the central bus with the most installed memory, the smallest HPA in the case of a tie in installed memory, and at least 256 Kbytes of memory.

Initial Memory Module Candidate (IMMC)

The **Initial Memory Module Candidate** or **IMMC** is a memory module on the central bus which has been selected by PDCE_RESET as a possible candidate for the Initial Memory Module. The Initial Memory Module Candidate must be successfully tested and initialized before it can be chosen as the Initial Memory Module. In addition, during powerfail recovery, PDCE_RESET must verify that the IMMC is the same memory module that was identified as the Initial Memory Module during the most recent boot.

Initial Program Load (IPL)

Initial Program Load or **IPL** is the first code loaded into memory from the boot device during boot.

Initial System Load (ISL)

Initial System Load or **ISL** is a standard code module used during the startup of any Precision operating system to provide a standard user interface during boot. On some systems this code may be the Initial Program Load (IPL), while on others IPL may perform some preliminary tasks and then load ISL.

I/O Address Space

The **I/O Address Space** is the range of addresses 0xF1000000 00000000 through 0xFFFFFFFF FFFFFFFF.

I/O-Dependent Code (IODC)

I/O-Dependent Code or **IODC** provides a uniform mechanism to obtain module-type dependent information from a module. IODC is composed of data bytes that identify and characterize the module and a set of entry points used to perform module-type dependent operations.

Keyboard Device

The **Keyboard Device** or **keyboard** is the input device that PDC uses during boot to obtain responses from the operator.

Local Broadcast Address Space

The **Local Broadcast Address Space** consists of addresses in the range 0xFFFFFFFF FFFC0000 through 0xFFFFFFFF FFFDFFFF. If an operation is sent to a register in the local broadcast address space, it applies to all modules on the local bus which implement that register.

Local Power Failure

A **local power failure** is a power failure which affects the central bus.

Logical Interchange Format (LIF)

The **Logical Interchange Format** or **LIF** is a standard format for mass storage implemented by many HP computers to assist in information and media transportability. The initial program load (IPL) code is stored in LIF format on the boot device.

Low-Priority Machine Check (LPMC)

A **Low-Priority Machine Check** or **LPMC** is the fifth highest priority interruption in a native processor. An LPMC indicates the detection of a hardware fault that has been recovered from without software intervention.

Memory Address

A **Memory Address** is an address in the memory address space.

Memory Address Space

The **Memory Address Space** consists of addresses in the range 0x00000000 00000000 through 0xEEFFFFFF FFFFFFFF.

Memory-Mapped I/O

In a **Memory-Mapped I/O** system, all communication with devices is done by load and store instructions to I/O registers that logically control the device. The registers function like memory locations, as far as software is concerned.

Memory Module (Memory)

A **Memory Module** or **Memory** is a module which responds to addresses within some subset of the memory address space and can be used to store and retrieve information (data and instructions) at these addresses.

Module

A **module** is an entity which is configured into the system address space and adheres to the Precision I/O Architecture. As the I/O system is memory-mapped, a module can be interrogated and controlled by software via the standard load and store instructions rather than with special I/O instructions. There are up to 64 modules per bus.

Module Set

A **Module Set** is a group of two or more modules completely contained on a single card.

Module Type

Each module and pseudo-module in a Precision Architecture system has a type associated with it. This type is stored in the module's IODC ROM in the IODC_TYPE byte.

Module Type Dependent

An item in a module is **Module Type Dependent** if its functional definition is dependent on the module's type, which is stored in the IODC_TYPE byte of the module's I/O-dependent code (IODC).

Monarch Processor

The **Monarch Processor** is the native processor which has been selected to perform boot, and execute IPL.

Monarch Selection

Monarch Selection is the process in which all the native processors compete for selection as the monarch processor.

Multi-module Card

A card containing a module set is a **Multi-module Card**.

Native Processor Module

A **Native Processor Module** is a processor module which executes the complete Precision instruction set and can execute standard operating system software.

Non-Volatile Memory (NVM)

Non-Volatile Memory or **NVM** is an optional system-wide resource used to store system configuration parameters during power failures. NVM is accessible through the PDC_NVOLATILE procedure. Unlike stable storage, NVM must have an unlimited lifetime write-cycle limit.

Normal Power Failure

A **normal power failure** is the situation in which the failure of primary power is preceded by a warning which allows enough time for the system to save its state in memory. Primary power is lost, but secondary power remains intact until primary power is restored. The system is able to reestablish its state during powerfail recovery and continue operation.

Operating System (OS)

The **Operating System** or **OS** is the supervisory software which controls user tasks and manages system resources.

Optional

A register or other facility or mechanism that is not required to be implemented in all cases is called **Optional**. Note that optionality is, in some cases, determined by things such as system configuration, rather than by free choice. For instance, the registers which provide I/O-dependent code functionality (IO_DC_ADDRESS and IO_DC_DATA) are optional, yet they are specifically required if the system configuration is not fixed at manufacturing time.

Page

A **Page** is a 4 Kbyte aligned, 4 Kbyte address range anywhere in the system address space.

Page Zero

The first page of memory is referred to as **Page Zero**. Thus Page Zero is comprised of addresses 0x00000000 00000000 through 0x00000000 00000FFF.

Physical Page Directory (PDIR)

The **Physical Page Directory** or **PDIR** is a table which contains the translations of all virtual addresses to their corresponding addresses. The PDIR is used to update the translation lookaside buffer (TLB) after the translation for any virtual address is not found in the TLB.

Powerfail Budget

Powerfail Budget is the minimum time that each bus specification guarantees between the assertion of BUS_POW_WARN and the deassertion of BUS_POW_VALID.

Powerfail Warning

A **Powerfail Warning** is a warning about an impending loss of bus power. It is indicated by the assertion of the BUS_POW_WARN signal.

Precision System (System)

A **Precision System** or **System** is the hardware consisting of one or more processors, memory, and I/O as configured for an application.

Primary Memory Module

A **Primary Memory Module** is a processor-dependent memory module with IODC_SPA[shift] greater than zero.

Primary State

Primary State is defined to be that state whose soft power-on value is either Constant, Random, or Defined. If Defined, the state must be a function of primary state and secondary or tertiary state. Primary state may be lost when BUS_POW_VALID is deasserted.

Privileged Page

All module actions which can produce security violations are restricted to **privileged pages**.

Programming Note

A **Programming Note** points out information of primary interest to software designers.

Processor-Dependent Code (PDC)

Processor-Dependent Code or **PDC** provides a uniform context in which to perform processor-dependent operations. PDC is comprised of a software entry point which provides a variety of options to execute specific procedures and a set of entry points that are triggered when special events are recognized by the processor module.

Processor-Dependent Interleave Group

A **Processor-Dependent Interleave Group** consists of exactly one primary memory module and zero or more satellite memory modules.

Processor Internal Memory (PIM)

Processor Internal Memory or **PIM** is a storage area in a processor that is set at the time of an HPMC, LPMC, Soft Boot, or TOC, and is composed of the architected state save error parameters, and HVERSION-dependent regions. The internal structure of PIM is HVERSION dependent. The PDC_PIM procedure is used to access PIM.

Processor Module (Processor)

A **Processor Module** or **Processor** is a native processor module.

Rendezvous

Rendezvous is the state in which all non-monarch processors wait while the monarch processor performs the boot process. A processor leaves rendezvous when it receives a rendezvous interrupt (interrupt to EIR{0}) from the monarch processor.

Repeated Power Failures

During **repeated power failures**, primary power is lost and regained many times in quick succession. The interval between failures is not sufficient to allow powerfail recovery to be completed before the next failure occurs. This mode of power failure may occur when the external power is just at the threshold needed for normal operation. All recovery algorithms are structured to recover successfully in the event of repeated power failures.

Reserved

A facility, address, or functionality is **Reserved** if it currently has no defined function in the Precision I/O Architecture but is restricted from current unarchitected uses because it is expected to be used for expansion of the architecture in the future.

Restart Execution

When a caller **restarts execution** of an entry point following an interruption, execution begins at the start of the entry point.

Resume Execution

When a caller **resumes execution** of an entry point following an interruption, execution begins at instruction i+1, where i was the last instruction executed in the entry point prior to the interruption.

Satellite Memory Module

A **Satellite Memory Module** is a processor-dependent memory module with IODC_SPA[shift] equal to zero.

Secondary State

Secondary State is defined to be that state whose soft power-on value is Unchanged and whose hard power-on value is Constant, Random, or Defined. If Defined, the state must be a function of secondary and tertiary state. Secondary state is independent of BUS_POW_VALID.

Simplex Console

A **Simplex Console** is a console where different I/O devices, and possible different I/O modules, are used for the console input and output functions.

Soft Boot

A **Soft Boot** is a boot in which memory is tested nondestructively to preserve as much of the system state as possible for later dump and analysis. A soft boot is initiated by a failed TOC.

Soft Physical Address (SPA)

The **Soft Physical Address** or **SPA** of a module is an additional range of addresses (other than its hard physical address or HPA) to which the module responds. A module's SPA space may reside in either the system's memory or I/O address space (but not both).

Software Version (SVERSION)

For each module, the **Software Version** or **SVERSION** specifies a unique module architecture. The *model* field of SVERSION specifies the software interface and is changed for implementations with incompatible software requirements. The *rev* field is changed when an enhanced architectural feature is added to the module. The *opt* field is module-type dependent. For native processors, SVERSION is returned by PDC_MODEL. For all other modules, SVERSION is stored in the IODC_SVERSION word of IODC.

Stable Storage

Stable Storage is a required system-wide resource used to maintain critical system parameters during power failures. Stable storage is accessible through the PDC_STABLE procedure.

Starvation

Starvation occurs when a module cannot obtain one or more of desired resources.

Storage Error

Storage errors occur when a module detects that portions of its data have become damaged. Storage errors are detected only if the module stores redundant check bits along its data. Data may become damaged in two ways: it may become invalid or it may become corrupt.

Storage Integrity

Storage Integrity is preserved if all stores up to some (possibly unspecified) point have been performed, and no stores at that point or beyond have been performed. If a store prior to the point was not done correctly, but the location is tagged such that subsequent accesses will result in a failed operation, then the store is still considered performed.

Sudden Power Failure

Sudden power failure is the situation in which the power system suffers a major hardware fault, and primary power is lost with no warning whatsoever. This is a catastrophic failure, since processor state cannot be preserved. When power is restored, the system will boot. The same effect will be achieved if power is preceded by a warning, but the interval is not long enough for the system to save its state.

Support Note

A **Support Note** points out information of primary interest to support.

SVERSION Dependent (SV)

An item in a module is **SVERSION Dependent** if its functional definition is dependent on the module's IODC_SVERSION[model] and IODC_SVERSION[rev]. The SVERSION designers are free to define the functionality, provided the definition does not conflict with any architected/module-type dependent definition, or to delegate definitional responsibility to the HVERSION designers.

System Address Space

The **System Address Space** consists of the entire address space of a Precision system and is in the range 0x00000000 00000000 through 0xFFFFFFFF FFFFFFFF.

System Operation

A **System Operation** or **Operation** is the term used to describe the data or control transfer taking place between one module, the system requestor, and one or more modules, the system responder(s), in a system.

Tertiary State

Tertiary State is defined to be that state which is neither primary state nor secondary state. Tertiary state is independent of both BUS_POW_VALID and BUS_SEC_VALID (i.e., the soft and hard power-on value of tertiary state must be Unchanged).

Third Party

A **third party** is a module which, although not explicitly addressed in a bus operation, is required to participate in coherent bus operations.

Timeout Error

A **Timeout Error** occurs when one party in a transaction does not perform some action within a specified amount of time.

Total Power Failure

A **total power failure** is the case in which all busses in a system lose primary power at about the same time. Provided that secondary state was maintained, recovery can start as soon as the central bus regains power. When all busses regain power, the entire system must be reinitialized.

Transaction

A **Transaction** is the indivisible primitive that a module, the master, uses to communicate with zero or more modules, the slave or slaves, on the same bus.

Transaction Buffer

Transaction Buffers hold transactions for which the operations have not yet been completed.

Translation Lookaside Buffer (TLB)

A **Translation Lookaside Buffer** or **TLB** is a hardware table which serves as a cache for virtual to memory address translation. When a memory reference is made to a given virtual address, the virtual page number is passed to the TLB and the TLB is searched for a matching entry. If the entry exists, the page number (contained in the entry) is concatenated with the page offset from the original virtual address to form a 32 bit address. If the entry does not exist, the TLB is updated from the page directory (PDIR). This latter condition is called a **TLB Miss**.

Uncacheable Page

An **Uncacheable Page** is a page which must be accessed with only non-burst operations. All pages in the I/O address space are uncacheable. The implementation of uncacheable pages in the memory or PDC address spaces are separate processor HVERSION dependent options.

Unprivileged Page

An **Unprivileged Page** is a page in which no access to that page can affect system security. For example, attempted access to an non-readable or non-writeable I/O register in an unprivileged page must not cause an access to an privileged page or cause a bus error.

Valid

A state, value, or action is **Valid** if, on a read, the data returned has its architected meaning, and on a write, the value written causes the architected effect.

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